

Attorney Docket #: N1085-00018(TSMC2002-0629)
Application Serial No.: 10/730,533
TC/AU No.: 1756
Amendment dated March 8, 2007

Amendments to the Specification:

Please amend the Title at page 1, line 1, of the Application as follows:

**CLEAR FIELD ANNULAR EQUAL LINE SPACE CHROMELESS PHASE SHIFTING
MASK AND METHODS FOR MANUFACTURING THE SAME**

Please amend Paragraph [0030] of the Specification as follows:

On the other hand, in order to form equal-line-space interconnect lines 520, 530, and 540, 550, 560, and 570 on a semiconductor substrate such as a wafer, corresponding lines 640, 650, 660, 670, 680, and 690 on a mask have to be positively biased. Lines 640, 650, [[and]] 660, 670, 680, and 690 are of a phase approximately 180 degrees different from the mask substrate 600.

Please amend Paragraph [0008] of the Specification as follows:

A mask comprises a mask substrate and at least one annular equal line space phase shifting pattern on said mask substrate to produce an opaque unexposed region on a semiconductor substrate. A method of manufacturing a mask comprises providing a mask substrate; forming a layer of resist material on said substrate; patterning at least one annular equal line space phase shifting pattern on said resist layer; patterning said pattern onto said mask substrate; removing a remaining portion of said resist layer. A method of transferring a pattern onto a semiconductor substrate comprises illuminating a mask comprising at least one annular equal line space phase shifting pattern on the mask to produce an opaque unexposed region on a semiconductor substrate.

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Please amend Paragraph [0019] of the Specification as follows:

The pattern 110 is an annular equal line space phase shifting structure that comprises annular rings 120, 130, 140, and a central portion 150. The outermost annular ring 120 has a phase shift of approximately 180 degrees from the mask substrate 105. The inner annular ring 130 has a phase shift of approximately 180 degrees from the outermost ring 120. Likewise, the innermost annular ring 140 has a phase shift of approximately 180 degrees from the inner annular ring 130 and the central portion 150 has a phase shift of approximately 180 degrees from the innermost annular ring 140. That is to say, phases of adjacent annular rings shift 180 degrees and phases of alternate annular rings are the same. In summary, annular rings 120 and 140 have the same phase, for example π (180 degrees). The mask substrate 105, annular ring 130, and the central portion 150 have the same phase, for example 0 degrees, that is 180 degrees different from that of annular rings 120 and 140.

Please amend Paragraph [0023] of the Specification as follows:

The pitch (P_m) on a mask substrate is N times of the corresponding pitch (P_s) on a semiconductor substrate where N can be an integer equal to or larger than one. For example, a four times (4X) mask is used in a stepper for photolithography processes, i.e. $P_m = 4P_s$. In order to form a large opaque unexposed region on a semiconductor substrate, there is no requirement of minimum mask pitch (P_m) for the annular equal line space phase shifting pattern as long as photolithography technology allows. As a result, a mask pitch (P_m) smaller than the corresponding critical dimension pitch on a semiconductor substrate ($N \times P_{cs}$, for example $4P_{cs}$) can result to a large opaque unexposed region on a semiconductor substrate. However, the mask pitch (P_m) of an annular equal line space phase shifting pattern has to be smaller than two times of the corresponding critical dimension pitch on a semiconductor substrate ($N \times 2P_{cs}$, for example $8P_{cs}$), in order to form a large opaque unexposed region on a semiconductor substrate. That is to say, $0 < P_m < N \times 2 P_{cs}$.

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Please amend Paragraph [0028] of the Specification as follows:

However, when an incident radiation 470 passes an annular equal line space phase shifting pattern where $N \times P_{cs} < P_m < N \times 2P_{cs}$, 0 order 480 of the diffraction disappears and only +1 order 482 of the diffraction enters a projection lens 440 to form an image. Because the intensity of +1 order 482 of the diffraction alone is much lower than a threshold exposure intensity, the portion of resist underlying an annular equal line space phase shifting pattern is not exposed. In another embodiment, when a mask pitch (P_m) is smaller than the corresponding critical dimension pitch on a semiconductor substrate ($N \times P_{cs}$, for example $4P_{cs}$), i.e. $P_m < N \times P_{cs}$, not only 0 order of the diffraction disappears but +1 order of the diffraction is also not collected by a projection lens. As a result, a large opaque unexposed region on a semiconductor substrate can be obtained. An opaque unexposed region that corresponds to the annular equal line space phase shifting pattern is then formed on the resist layer 450 and further transferred to the semiconductor substrate 460. Without employing an annular equal line space phase shifting pattern, a large feature such as a pad or an interconnect would be exposed to a ring-like shape with a hollow inside rather than a solid shape that the feature is designed to be. Thus, when a sufficiently large feature, depending on the photolithography environment, begins to be exposed as a hollow ring rather than a solid dark region on a semiconductor substrate, an equal line space phase shifting pattern can be applied to the large interconnect to improve the result of exposure.

Please amend Paragraph [0029] of the Specification as follows:

As shown in FIG. 5, an integrated circuit design on a semiconductor substrate 505 usually contains a larger interconnect area 510 and thinner interconnect lines 520, 530, 540, 550, 560, and 570. A phase shifting mask capable of transferring a pattern containing both large opaque unexposed areas 510 and features with critical small dimension 520 to 570 is necessary. As mentioned above, a chromeless phase shifting mask with an annular equal line space phase shifting pattern thereon can be employed to transfer an opaque uncxposed region onto a semiconductor substrate such as a wafer. Thus, to form a larger interconnect area 510 on a wafer, an annular equal line space phase shifting pattern 605 on a mask comprising annular rings

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610, 620 and a central portion 630 as shown in Fig. 6 is used. The annular ring 610 and the central portion 630 are at the same phase, which is approximately 180 degrees different from that of the annular ring 620 and of the mask substrate 600.